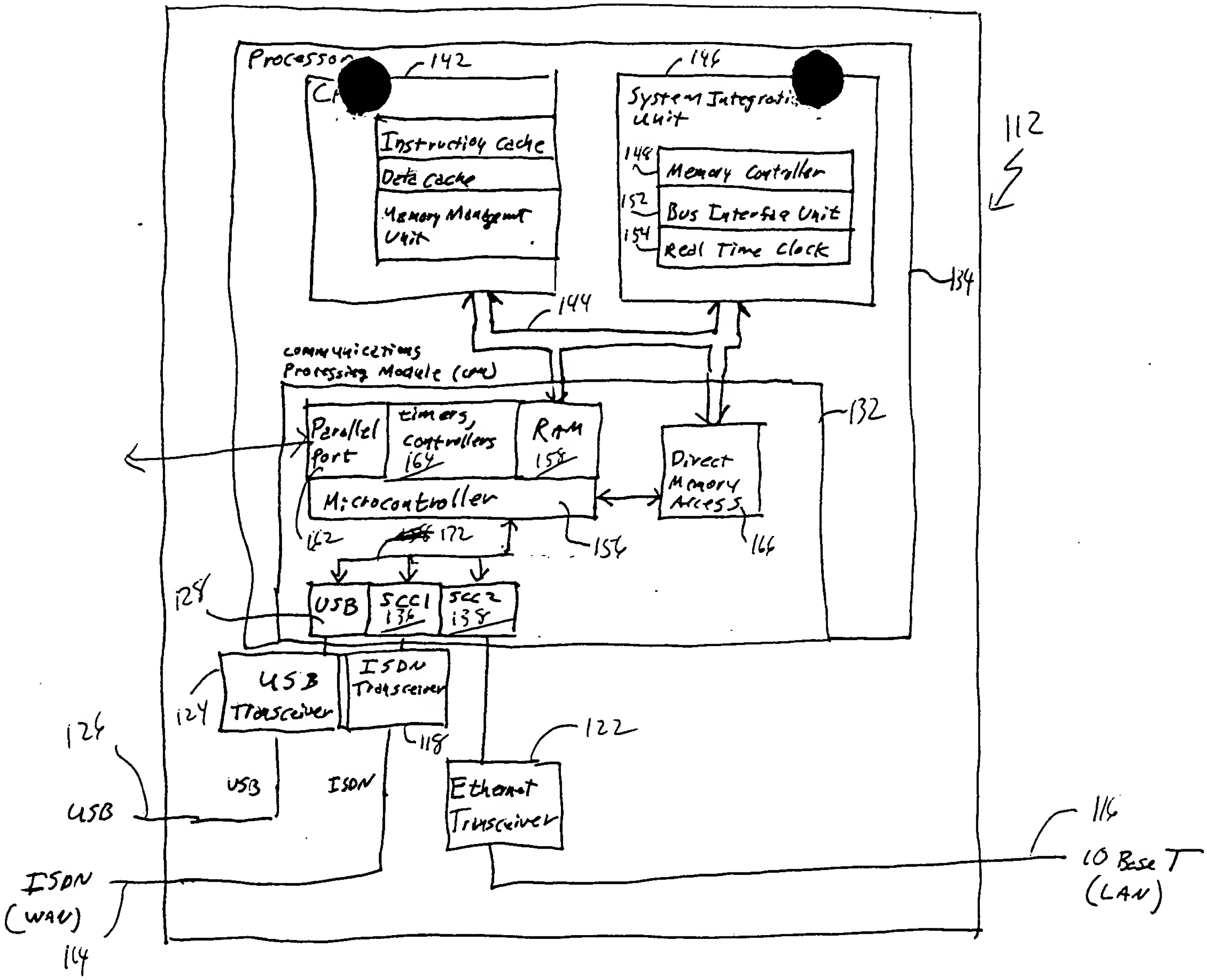

142
146
112
Instruction cache
Data cache
Memory Management Unit
unit
148
Memory Controller
152
Bus Interface Unit
154
Real Time Clock
134
144
Communications Processing Module (CPM)
132
Parallel port
timers, controllers 164
RAM 158
Microcontroller
Direct Memory Access
162
172
156
166
128
USB
SCC1 136
SCC2 138
USB Transceiver
ISDN Transceiver
124
118
126
122
USB
USB
ISDN
Ethernet Transceiver
116
10 Base T (LAN)
ISDN (WAN)
114

Fig 1

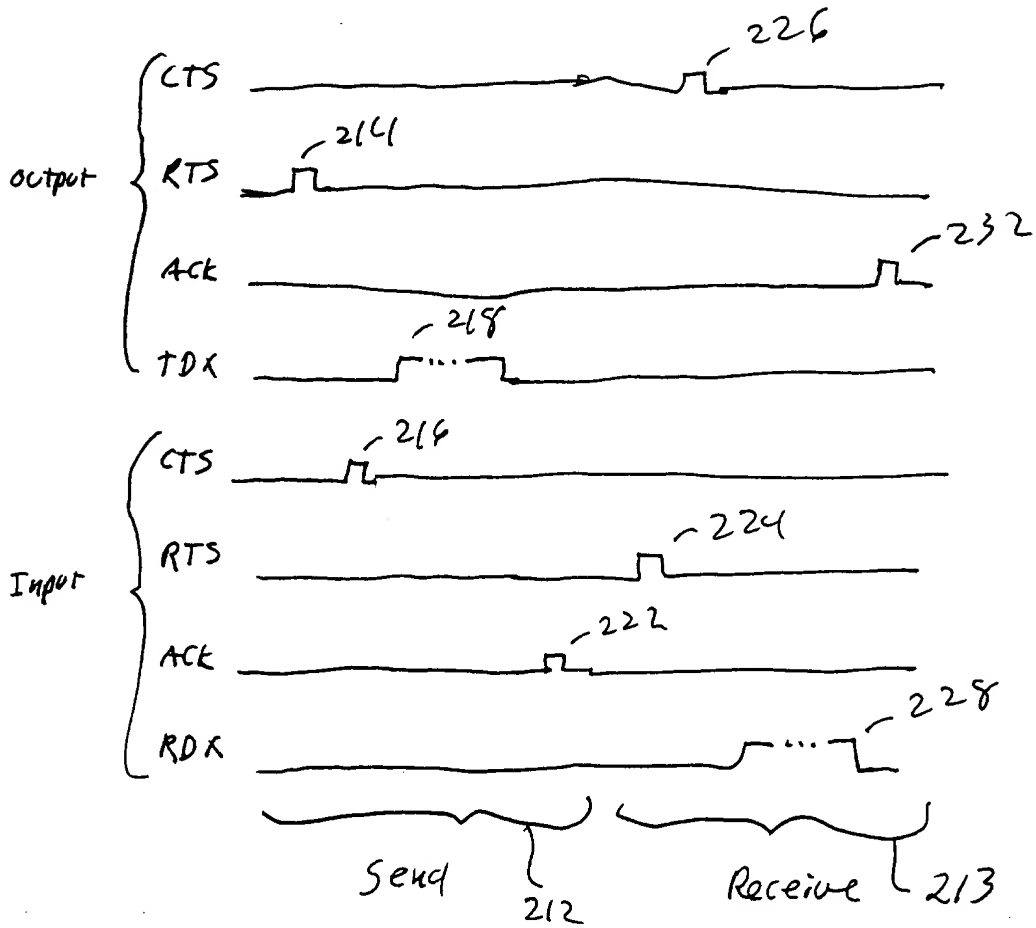


Fig 2 Prior Art

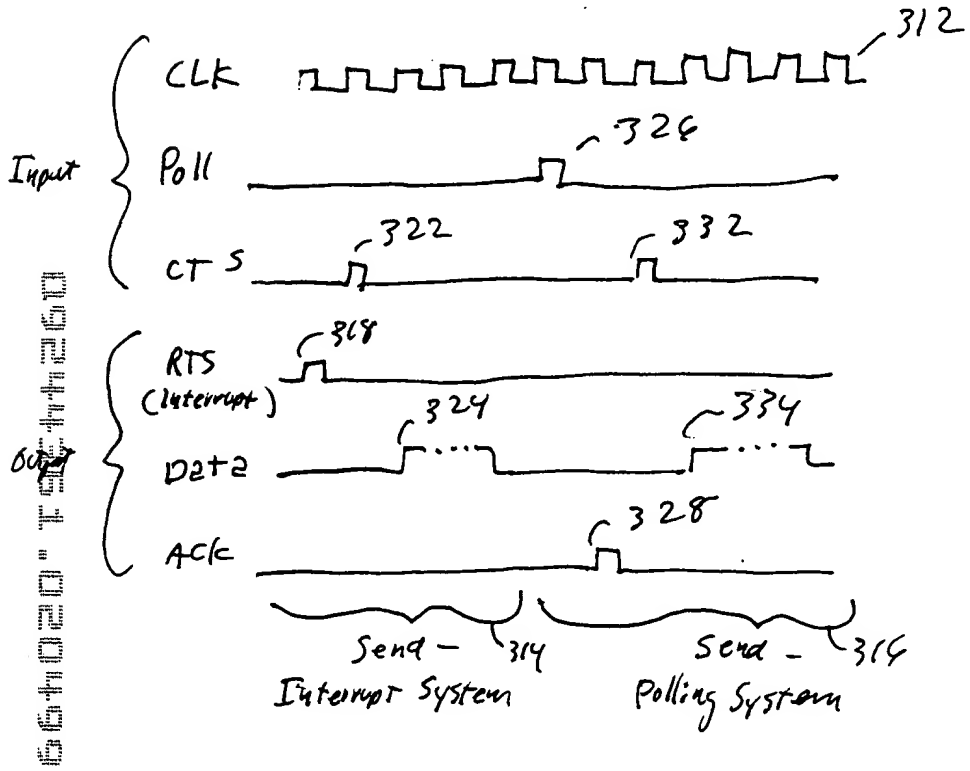


Fig 3 Prior Art

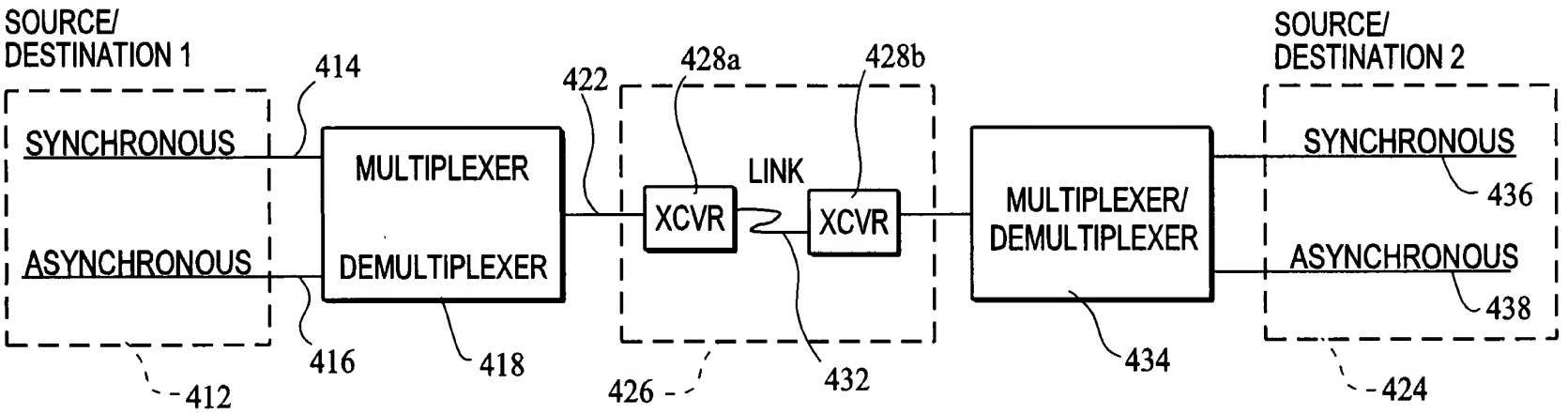


FIG. 4

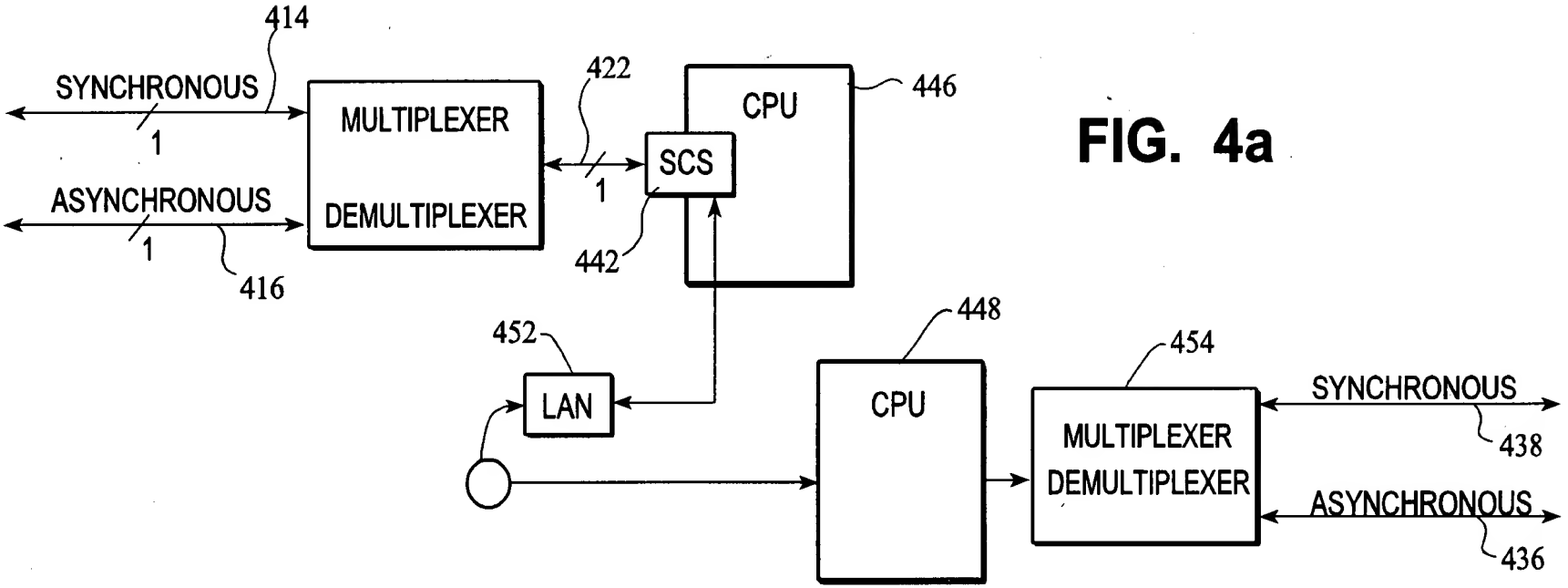


FIG. 4a

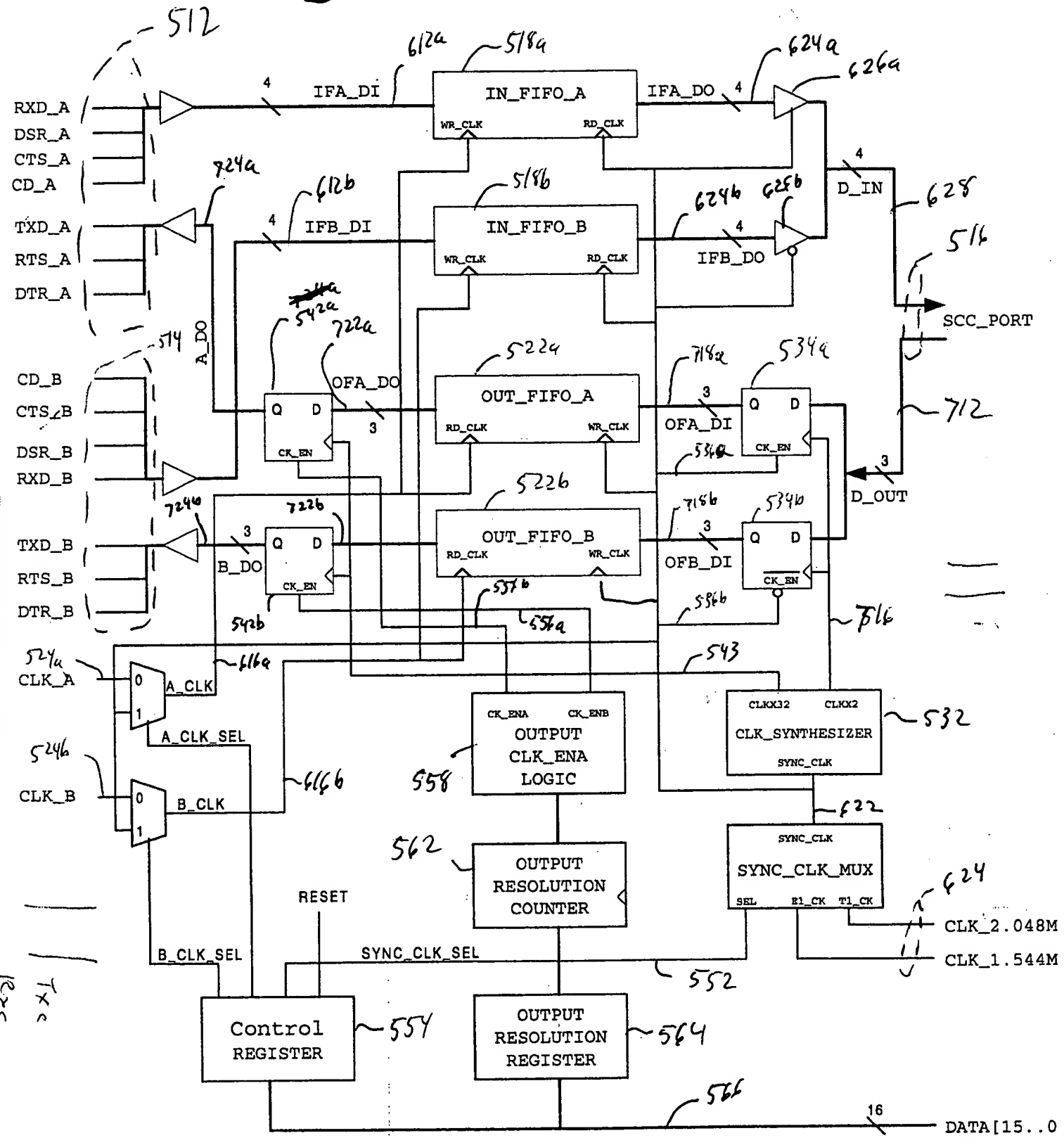


Fig. 5

BLOCK GIAGRAM : TDM OF ASYNCHRONOUS DATA STREAMS

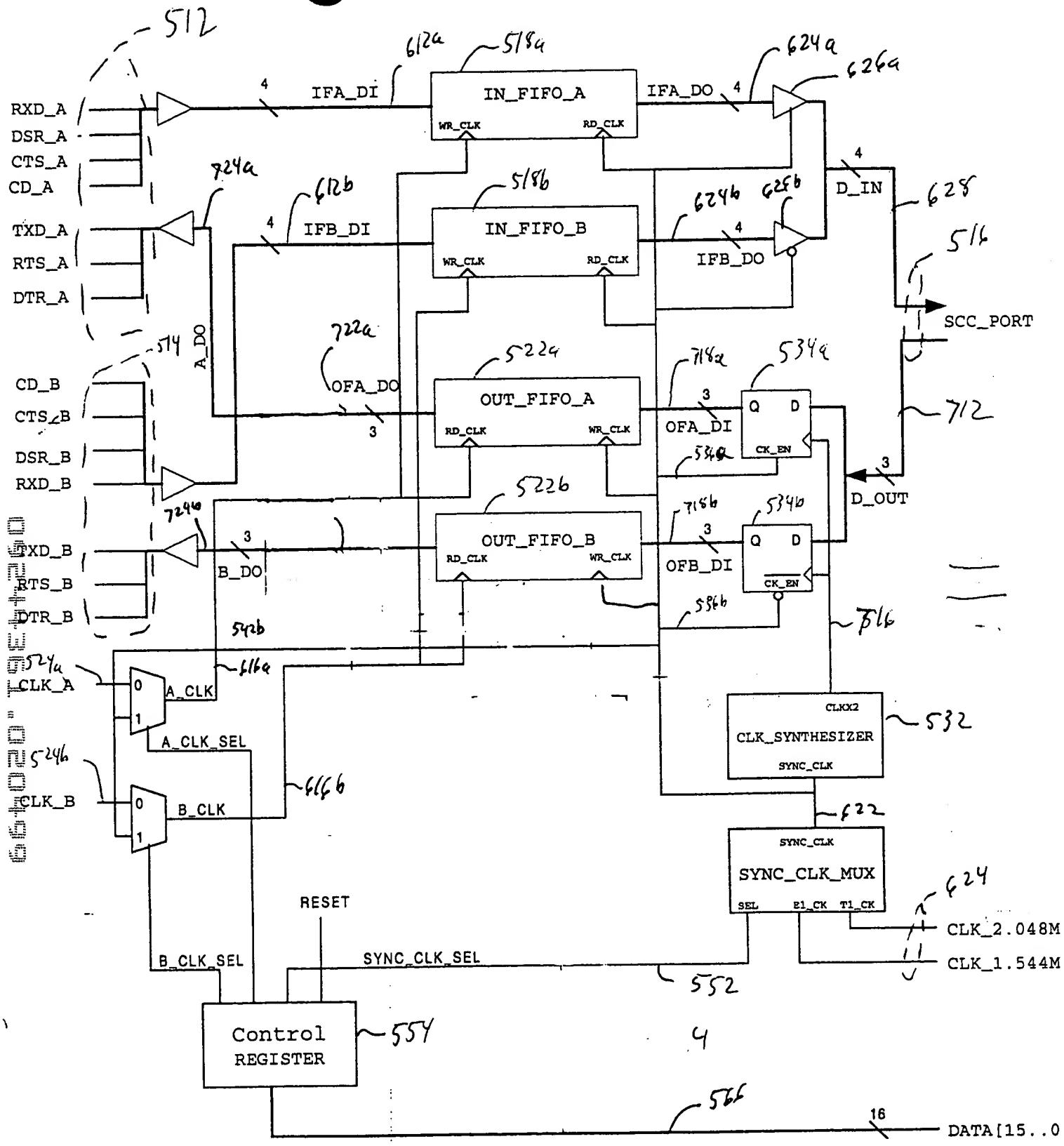
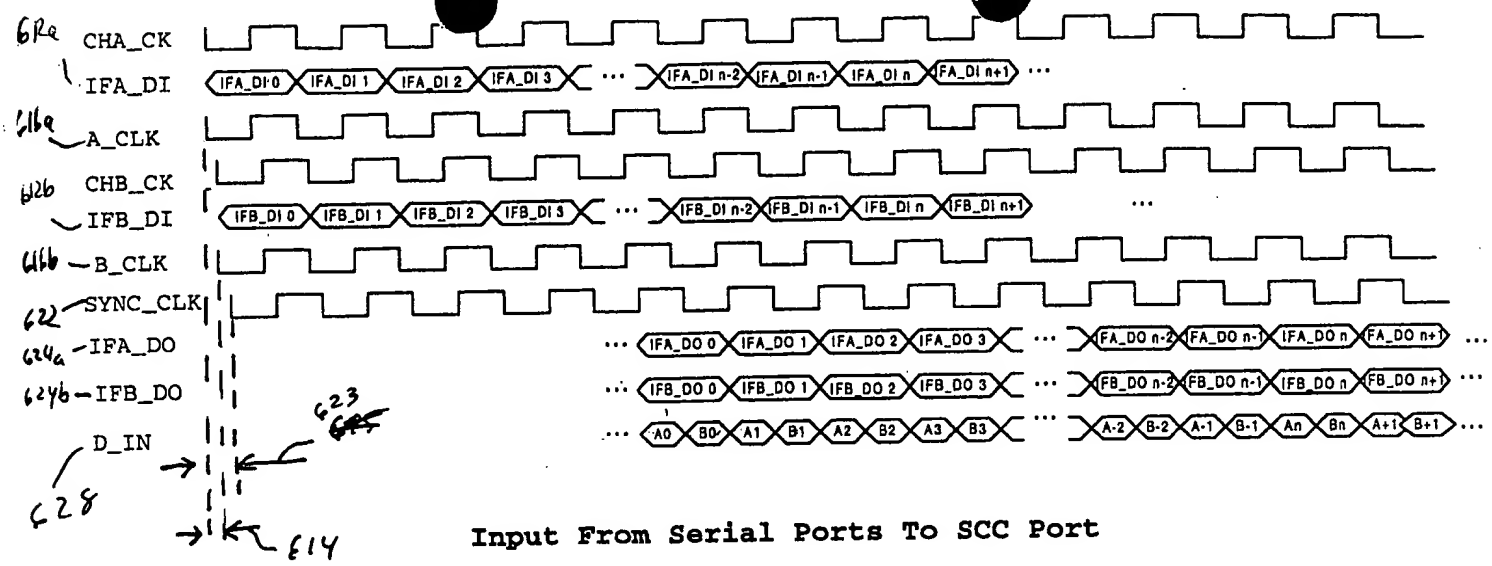


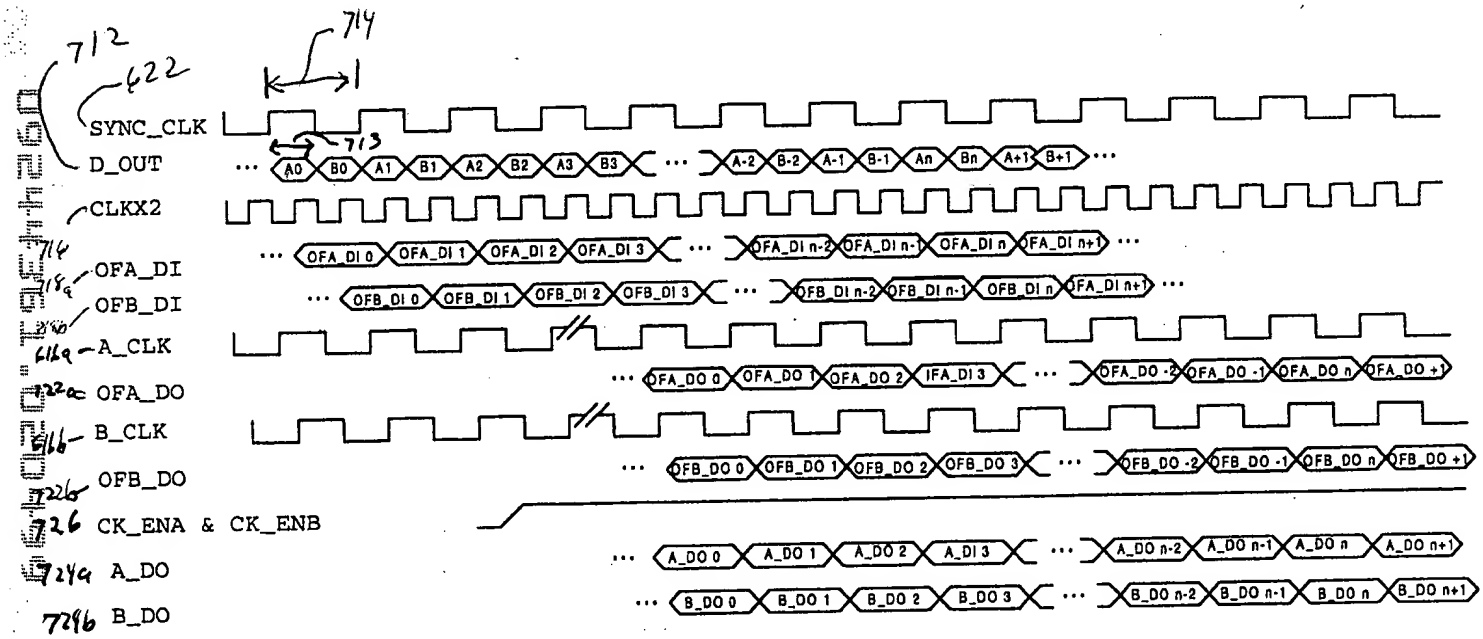
Fig. 5A

BLOCK DIAGRAM : TDM OF ASYNCHRONOUS DATA STREAMS



Input From Serial Ports To SCC Port

Fig 6



Output From SCC Port To Serial Ports

Fig 7

Case 1 : 2 Synchronous Channels with Same Clock Rate but Clock Skews

Fig 8

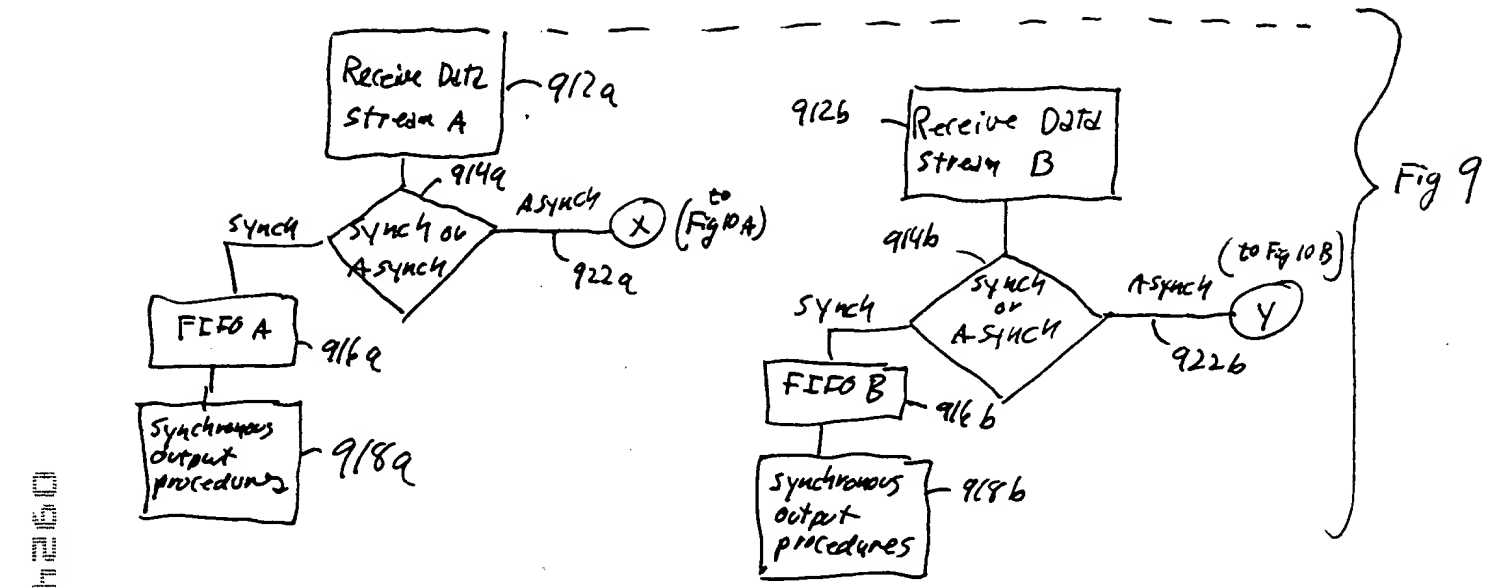


Fig 9

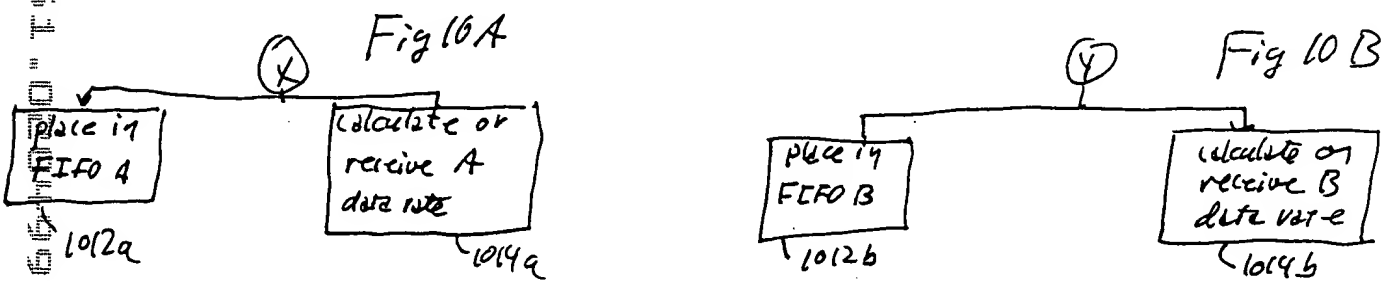


Fig 10A

Fig 10B

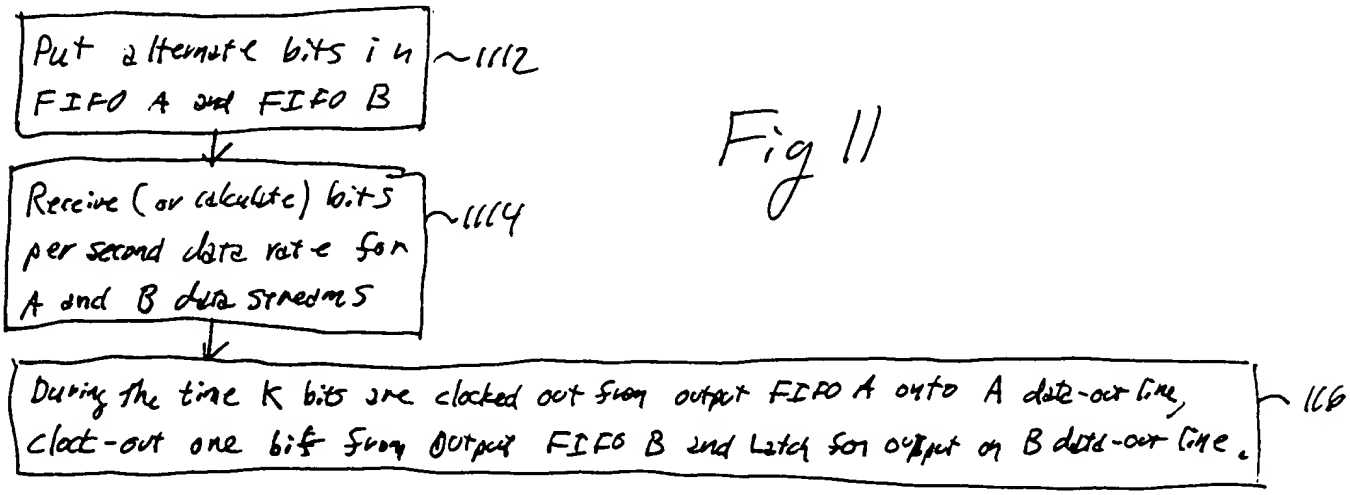


Fig 11

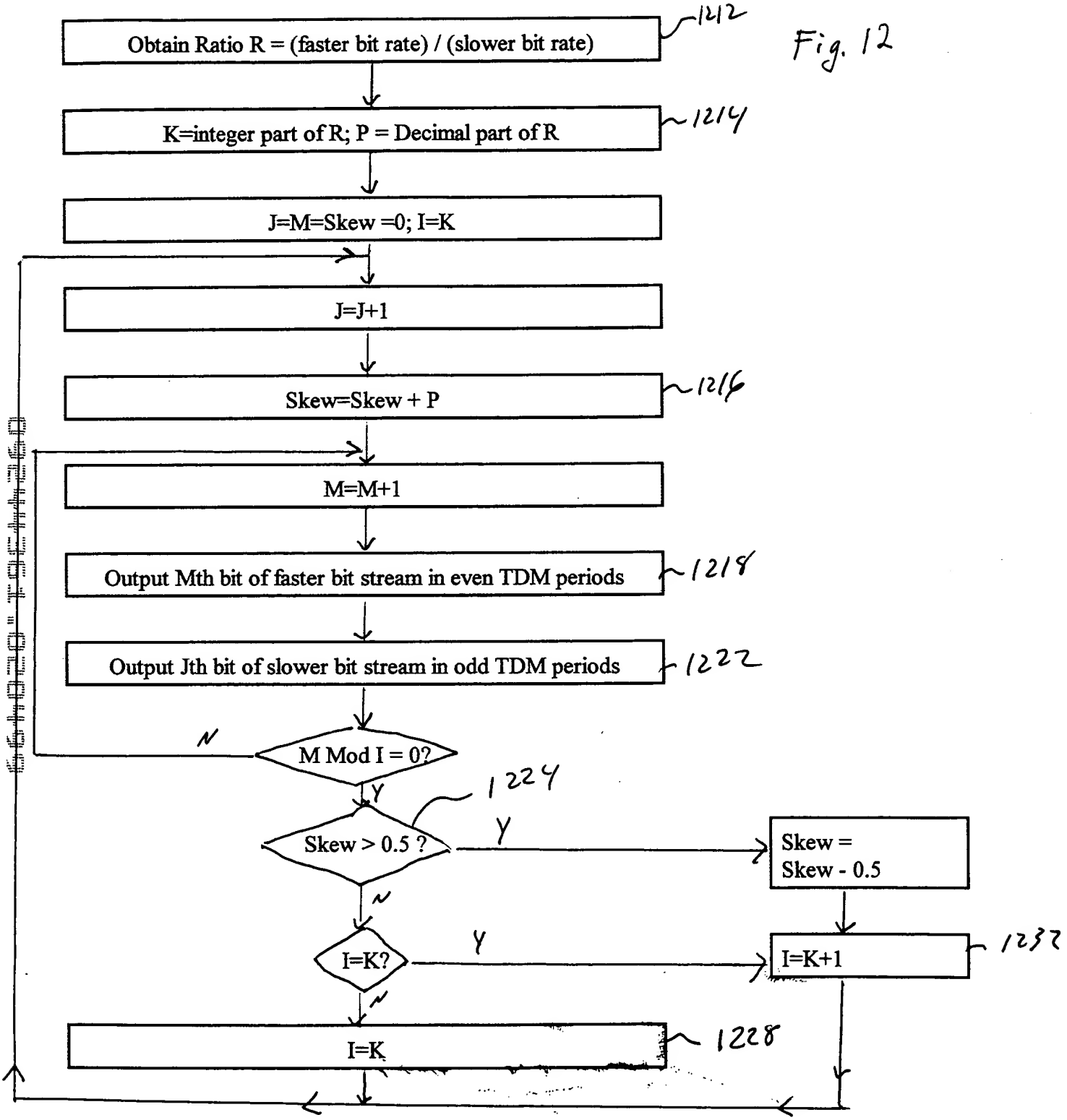


Fig. 12

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